Gabriel Weisz

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Citizenship: United States of America

Education

PhD **Carnegie Mellon University, Department of Computer Science**.
Thesis defense planned for August 2015
Advisor: James C. Hoe
Thesis Title: CoRAM++: An Interface and Mechanism Efficiently Supporting Key Memory Access Patterns in FPGA Computing

M.S. **Carnegie Mellon University, Department of Computer Science**.
Awarded May 2013

B.S. **Cornell University, College of Engineering**, *Cum Laude*.
Double major in computer science and electrical engineering. Awarded May 1999.
Dean's list, spring 1996-spring 1999 inclusive.

Research Experience

2010–present **PhD Candidate**, *Computer Architecture Lab at Carnegie Mellon*, Carnegie Mellon University.

CoRAM++: CoRAM++: A Soft-Logic Abstraction for Accelerating Data Transfers Through a Library of Pattern-Specific APIs.

My thesis explores the idea that abstractions for FPGA computing should support libraries for complex data access patterns, and that these libraries should be able to instantiate logic near DRAM controllers to accelerate irregular data accesses.

FPGA computing applications have begun to target abstractions that provide data management services rather than directly interacting with DRAM controllers and communication interfaces. These abstractions ease the burden of manually orchestrating data transfers over DRAM controllers while also providing portability across devices, but have not focused on reusable code for complex data access patterns, and instantiate logic between application components and DRAM controllers, increasing latency and reducing performance when applications perform irregular, data dependent accesses.

Applications targeting the low-overhead CoRAM++ abstraction achieve over 96% of peak DRAM bandwidth when performing regular accesses. When supporting more complex data access patterns, CoRAM++ applications match the performance of reference applications while offering more flexibility and targeting a simpler programming model. Finally, CoRAM++ Agents placed near DRAM controllers portably improve the performance of CoRAM++ applications with irregular accesses by up to 5.2×.

GraphGen for CoRAM.

This project implements an optimizing FPGA back end for the GraphGen graph compiler. The GraphGen graph compiler converts a high level graph specification into an implementation for FPGA and GPU accelerators. The goal of the project is to allow graph application experts – rather than accelerator experts – to build high performance implementations their applications. I developed an optimizing FPGA back end to convert an intermediate representation of the graph application into one ready to be used of FPGA devices. This back end automatically optimizes memory accesses by the graph program, and is parameterized easily accommodate different data formats and on chip buffering requirements.

Intel Siskiyou on FPGAs.

I created an infrastructure to support Intel Siskiyou Peak processor cores on FPGAs. This included local instruction and data caches, schedule applications on individual cores on the FPGA, and ways for the processor core to access global FPGA DRAM. The infrastructure supported up to 8 processor cores running at 50 MHz on the Xilinx ML605, and 16 processor cores running at 100 MHz on the Terasic DE4 (with an Altera FPGA).

C-to-CoRAM.
In this project I created an high level synthesis tool that optimizes loop nests and uses the CoRAM architecture to implement DRAM accesses. The tool automatically optimizes loop nests for parallelism and data reuse, and instantiates smart stream buffers to implement data reuse patterns found by the compiler, reducing the DRAM bandwidth requirements of the application. The end result was that compiled computations were comparable to hand designs on the same FPGA board. During this project, I implemented several important pieces of the CoRAM architecture, including support for staging data between a host PC and FPGA, benchmarking applications on the FPGA, and hardware support for the Terasic DE4 board with an Altera FPGA.

1995–1999 **Undergraduate Research**, Cornell University.

Concurrent Hardware Process Simulator.
Under the supervision of Rajit Manohar, I built a program to convert a Concurrent Hardware Processes description of a program into a multithreaded software simulation.

3D Chess Game.
Under the supervision of Bruce Land, I built a computer version of the 3d multilevel chess game from Star Trek. This game was designed to provide a 3d experience on systems with Pentium class CPUs (and no GPU), and ran on both Windows and Linux using OpenCL. It supported both one and two player operation. and incorporated a computer AI based on GNU Chess.

Teaching Experience

Fall 2012 **Teaching Assistant**, *Introduction to Computer Systems*, Carnegie Mellon University.

Spring 2012 **Teaching Assistant**, *Graduate Compilers*, Carnegie Mellon University.

Spring 1998 **Undergraduate Teaching Assistant**, *Computer Organization, Computer Graphics, Introductory Computer Programming*, Cornell University.

Fall 1997 **Undergraduate Teaching Assistant**, *Introductory Computer Programming*, Cornell University.

Spring 1997 **Undergraduate Teaching Assistant**, *Introductory Computer Programming*, Cornell University.

Professional Experience

1999-2010 **Co-founder and Vice President of Technology**, *Salar, Inc.*

- Bootstrapped the company from startup to millions of dollars in annual revenues, customers among the top hospitals in the country, and an award for Baltimore's best place to work in 2009 (micro category).
- Managed of the company's development team.
- Software architect and development team leader. Selected projects:
  - TeamNotes, Salar's flagship documentation and charge capture product, in use by over 25 hospitals for over a million patient record per year.
  - An embeddable version of the TeamNotes form engine that was licensed to several customers.
  - Referral+, an award winning referral management tool in use since 2007.
  - Tap, a Palm OS physician professional fee charge capture system.
  - The Palm OS version of the Johns Hopkins Antibiotic Guide, a handheld clinical drug reference that was been downloaded by over 150,000 people worldwide.
  - A document management system for creating peer reviewed medical references that publishes to the web, print, and mobile devices.
- Managed membership in the Microsoft Certified Partner program, including product validation and customer references.

1999 **Software Engineer**, *Immersive Technologies, LLC.*

Developer on the company's platform for creating cinematic, photo-realistic images using beam tracing techniques and a novel special subdivision algorithm, which were ultimately implemented in hardware.

1998–1999 **Software Engineer**, *Jump Networks.*

Developer on one of the first free web-based email, shared calendar, and contact management systems. I worked on the company's core platform, which was implemented as a custom Apache module, on syncing contact and other data between the desktop and web system, and on the email transport system.

Publications and Tutorials

FCCM 2014 Eriko Nurvitadhi, Gabriel Weisz, Yu Wang, Skand Hurkat, Marie Nguyen, James C. Hoe, Josè F. Martìnez, and Carlos Guestrin.
GraphGen: An FPGA Framework for Vertex-Centric Graph Computation
The 22nd IEEE International Symposium on Field-Programmable Custom Computing Machines, Boston, MA, May 2014

CARL 2013 Gabriel Weisz, Eriko Nurvitadhi, and James C. Hoe.
GraphGen for CoRAM: Graph Computation on FPGAs
The Third Workshop on the Intersections of Computer Architecture and Reconfigurable Logic,Davis, CA,December 2013 **(Presenter)**

FPGA 2013 Gabriel Weisz and James C. Hoe.
C-To-CoRAM: Compiling Perfect Loop Nests to the Portable CoRAM Abstraction
The 21st ACM International Symposium on Field-Programmable Gate Arrays,Monterey, CA,February 2013 **(Presenter)**

FPGA 2012 Eric S. Chung, Michael K. Papamichael, Gabriel Weisz, James C. Hoe, and Ken Mai.
Prototype and Evaluation of the CoRAM Memory Architecture for FPGA-Based Computing
The 20th ACM International Symposium on Field-Programmable Gate Arrays,Monterey, CA,February 2012

FPGA 2013 Eric S. Chung, Michael K. Papamichael, Gabriel Weisz and James C. Hoe.
Tutorial: Cross-Platform FPGA Accelerator Development Using CoRAM and CONNECT
The 21st ACM International Symposium on Field-Programmable Gate Arrays,Monterey, CA,February 2013

MICRO 2012 Eric S. Chung, Michael K. Papamichael, Gabriel Weisz and James C. Hoe.
Tutorial: FPGA Accelerator Development Using the CoRAM Virtual Architecture
The 45th Annual IEEE/ACM International Symposium on Microarchitecture,Vancouver, BC, December 2012

Patents, Awards, and Activities

2012 **Patent #8,326,653** Method and apparatus for analyzing patient medical records. Gottlieb, Gottlieb, & Weisz

2015 **Grand Awards Judge** Systems Software Category, Intel International Science and Engineering Fair

2013-Present **Member of the Board of Directors** Cornell Club of Pittsburgh

2012-Present **Member of the Doctoral Review Committee** Computer Science Department, Carnegie Mellon University

2012-2014 **Member of the PhD Program Admissions Committee** Computer Science Department, Carnegie Mellon University

2012 **Grand Awards Judge** Computer Science Category, Intel International Science and Engineering Fair

2011-Present **Undergraduate Admissions Contact** Cornell Alumni Admissions Ambassador Network

2010-Present **Graduate Fellowship** Computer Science Department, Carnegie Mellon University

2004–2005 **Team Mentor** Greater Baltimore Technology Council "Mosh Pit" Business Plan Competition

Skills

Technical leadership: System architecture, design, and development of thick client applications, mobile applications, web applications, enterprise and distributed systems, security infrastructure, and databases

Project management: Requirements gathering, specification development, timeline creation, testing and issue tracking, revision control, configuration and release management, code reviews

Programming languages: C, C++, C#, Java, JavaScript, SQL, Python, Perl, PHP, VB, Matlab, XML, HTML, Verilog, VHDL, Bluespec System Verilog

Development environments and technologies: Microsoft Visual Studio, Eclipse, gcc/make, .Net, MFC, ADO, COM, ODBC, DAO, ActiveX, OpenGL, DirectX

Databases: Microsoft SQL Server, Oracle, MySQL, Sqlite